# An Optimization Approach in Wafer Selection in a Assembly/Test Semiconductor Manufacturing Environment

**Lowell Lorenzo**
*Dept. of Industrial Engineering & Operations Research*
*Room 109 Melchor Hall, College of Engineering*
*University of the Philippines – Diliman*
*lowell.lorenzo@up.edu.ph*

Abstract

The phenomenon of circuit yield of fabricated wafers of integrated circuit chips in the manufacture of semiconductor devices in an assembly/test manufacturing environment is a major factor to consider in the attainment of high delivery reliability and minimum inventory levels of work-in-process during the production planning process at the shop floor. A mathematical programming model is developed to address this phenomenon with the aim of optimizing the selection of wafers of integrated circuit chips that will satisfy customer demand and at the same time yield the minimum number of semiconductor devices produced without orders due to the yield loss of the wafers. Validation of the mathematical model based on the results of a pilot project has demonstrated the efficiency of this optimization approach.